

# **Development of a Photothermal Reflectance Method for Microscale Thermal Resistance in SiP-Mounted Semiconductor Devices**

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Recently, a new method for implementation of high-performance semiconductor devices, called System in Package (SiP), has been developed. In this method, several LSI chips are densely stored in one package. So heat flux in SiP-mounted device is very high and precise thermal management is necessary. The purpose of our study is accurate evaluation of thermal resistance change on actual microscale structures in SiP-mounted device, due to structural degradation. The present study is focusing on a Flip-Chip junction structure which is a main route of heat removal in the device. The structure consists of several layers including a bump whose diameter and height are 70 microns and 30 microns, respectively. To measure interfacial thermal resistance between the layers, we have applied a periodic heating and thermoreflectance method. In this method, a sample is heated periodically and thermal properties of the sample are extracted from a phase-lag of temperature oscillation at the sample surface. By theoretical modeling of a measurement sample (Au-bump on Si-chip) and simulation, we verified that the phase-lag has adequate sensitivity to interfacial thermal resistance of the sample. Next, we developed a measurement apparatus. For heating the microscale region and detecting the temperature oscillation, laser diode and He-Ne laser is coincidentally focused on the sample surface by a condenser lens. Temperature detection at heated surface (called Front Surface Illumination; FSI) enables highly-sensitive measurement. Reflected He-Ne laser beam oscillating due to the surface temperature is guided to the detector. By scanning of Au-bump, we confirmed spatial resolution of the apparatus to be 10 microns. We also conducted a measurement using metal wafers which have known properties, verifying that the apparatus operates according to the measurement theory. Furthermore, we conducted a measurement using Au-bump, indicating that the apparatus has applicability to evaluation of thermal resistance on the Flip-Chip junction structure.